EXPRESS MAIL LABEL NO. EV381145615US

CLAIMS

1. A method for producing a flash memory comprising:

forming at least two adjacent rows of precursor stacks of floating gate transistors on a semiconductor substrate, with the precursor stacks being at least partially covered by a protective resin and being separated by a formation zone for a source line;

forming a trench in the formation zone for the source line by an attack of the formation zone and of the protective resin so as to result in a deposit of residue from the resin below the precursor stacks;

removing the residue deposit; and

implanting a source line in the formation zone below the precursor stacks.

2. The method of claim 1, wherein the forming a trench includes forming a trench which is the type having an SAS auto-aligned source.

3. The method of claim 1, wherein the forming a trench includes forming a trench so as to result in the protective resin formed from a thick DUV resin.

4. The method of claim 2, wherein the forming a trench includes forming a trench so as to result in the protective resin formed from a thick DUV resin.

5. The method of claim 1, wherein the forming a trench includes forming a trench so as to result in the protective resin formed of thick i-line resin.

6. The method of claim 2, wherein the forming a trench includes forming a trench so as to result in the protective resin formed of thick i-line resin.

7. The method of claim 5, wherein the forming at least two adjacent rows of precursor stacks of floating gate transistors on a semiconductor substrate includes forming a semiconductor substrate with a drain for each precursor stack,

wherein the drain is covered in a resin; and

wherein for each of the precursor stacks, the drain is formed opposite the formation zone for the source line.

8. The method of claim 6, wherein the forming at least two adjacent rows of precursor stacks of floating gate transistors on a semiconductor substrate includes forming a semiconductor substrate with a drain for each precursor stack,

wherein the drain is covered in a resin; and

wherein for each of the precursor stacks, the drain is formed opposite the formation zone for the source line.

9. The method of claim 1, wherein the removing the deposit of residue includes removing the deposit of residue by generating dioxygen plasma.

10. The method of claim 4, wherein the removing the deposit of residue includes removing the deposit of residue by generating dioxygen plasma.

11. The method of claim 6, wherein the removing the deposit of residue includes removing the deposit of residue by generating dioxygen plasma.

12. The method of claim 8, wherein the removing the deposit of residue includes removing the deposit of residue by generating dioxygen plasma.

13. The method of claim 1, further comprising:

removing the protective resin following implantation of the source line.

14. The method of claim 4, further comprising:
removing the protective resin following implantation of the source line.

15. The method of claim 6, further comprising:
removing the protective resin following implantation of the source line.

16. The method of claim 8, further comprising:
removing the protective resin following implantation of the source line.

17. The method of claim 12, further comprising:
removing the protective resin following implantation of the source line.

18. The method of claim 1, wherein the implanting the source line includes doping the source line with arsenic.

19. The method of claim 1, wherein the implanting the source line includes implanting the source line 25 nanometres out from an edge under a gate oxide of the precursor stacks.

20. A flash memory device comprising:

a semi-conductor substrate with an auto-aligned source line and fitted with at least two adjacent rows of floating gate transistors wherein the rows are separated by the source line; and

a gate oxide for each of the floating gate transistors, wherein the source line is implanted 25 nanometres off an edge under the gate oxide of the transistors.